

NbN A/I Conversion of IR Focal Plane Sensor Signal at 10 K

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Abstract-We are implementing a 12 bit SFQ counting ADC with parallel-to-serial readout using our established 10 K NbN capability. This circuit provides a key element of the analog signal processor (ASP) used in large infrared focal plane arrays. The circuit processes the signal data stream from a Si:AsBiB detector array. A 10 mega samples per second (MSPS) pixel data stream flows from the chip at a 120 megabit bit rate in a format that is compatible with other superconductive time dependent processor (TDP) circuits being developed. We will discuss our planned ASP demonstration, the circuit design, and test results.

1. INTRODUCTION

Very large focal plane arrays consisting of tens of thousands to over a million detector elements (pixels) in the visible to far IR electromagnetic spectrum are used for space based surveillance by the DoD and space and planetary exploration by the NASA. While great strides have been made, in the production of very large focal plane arrays, ever increasing performance requirements are being stipulated, in direct opposition to the growing demand for decreased systems costs. The DoD is moving toward smaller, lighter weight systems, e.g., lightsats, with dramatically lower launch costs while at the same time considering more complex, multi spectral imagery capability with its additional processing requirements. The NASA's continued probing of outer space will require an IR sensor capability extending to the very far infrared, tens to hundreds of microns, requiring detectors which operate at temperatures from a few Kelvin to sub Kelvin.

One type of surveillance systems requires cooling the detectors to 10 K using a cryocooler. We plan to demonstrate the feasibility of integrating a NbNADC with the cooled electronics, all at 10 K. Present sensor systems include the detector array, analog multiplexing and analog buffer amplifiers on the focal plane. As illustrated in Figure 1 for a surveillance system, the buffered focal plane analog signals are brought across a large temperature interface to the external analog to digital converter (ADC) and subsequent analog and digital signal processing.

For 10 K operation, more than a 1000 W of cooler power is required to remove each Watt of heat from the cold end. The heat from two primary sources must be removed

from the cold end: circuit dissipation, and signal line conduction. Using present technology the IR detector array dissipates between five and ten microwatts per pixel, mostly accrued by the analog buffer amplifiers which drive the output analog data lines. For a 10,000 pixel system, the focal plane dissipation is some forty milliwatts and the cooler plug power is a nominal 140 W, while for a megapixel system, costly kilowatts are required.

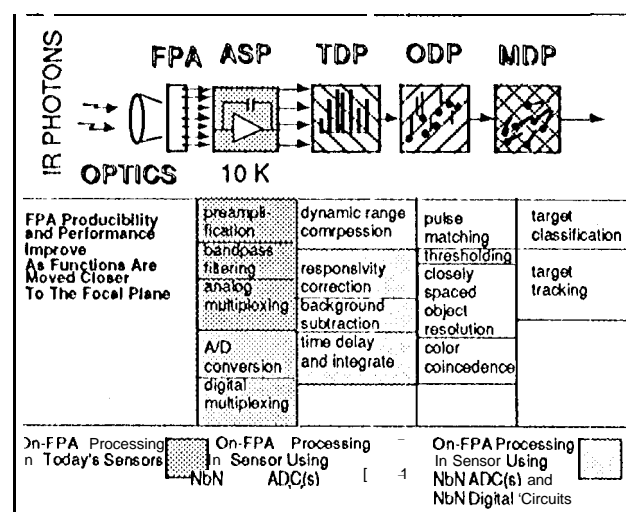


Figure 1: Focal plane array sensor systems presently only include the preamplifiers, bandpass filters, and analog multiplexers on the focal plane. Movement of the ADC and digital multiplexer will significantly improve manufacturability and performance.

A large portion of the conductive heat load is due to the signal cables. Reducing the heat load from these cables must be traded against the opposing need for high electrical conduction to minimize signal degradation of the low level analog signals. Additionally, the large number, often hundreds, of cables increases the system susceptibility to noise and becomes a labor intensive, costly manufacturability issue.

Placing the ADC on the focal plane significantly reduces the interface thermal load. The digital signals are more immune to noise contamination and additional data compression afforded by digital multiplexing on the focal plane reduces the interconnect cable count. While there has been some progress toward accomplishing this goal using semiconductor electronics, the added power dissipation adds hundreds of milliwatts to the cold end, hence hundreds of Watts to the system power generation and heat removal requirements.

A NbN, single flux quantum (SFQ), counting ADC similar to Nb versions reported previously, and a NbN

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version reported recently [1] can achieve the required conversion speed with an acceptable power dissipation. As summarized in Figure 2, the superconducting ADC's provide excellent performance in dynamic range and conversion rate at very low power. In contrast to semiconductor ADCs, where faster conversion rate results in higher power consumption, the superconductive ADC requires only a few microwatt, independent of operating speed,

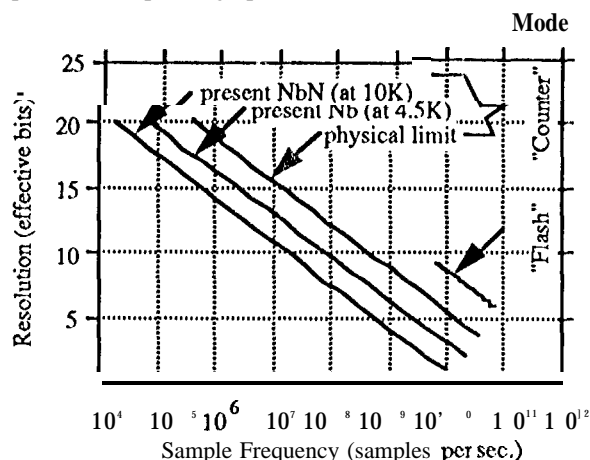


Figure 2: Superconductive ADC performance.

II. DEMONSTRATION TEST BED

JPL is assembling a test bed to demonstrate an ASP system including a superconducting A/D converter provided by TRW. The primary elements of the test bed, illustrated in Figure 3, include a Si:X focal plane array, focal plane array readout electronics, a multiplexer, a buffer to condition the FPA output for the A/D converter, and the A/D converter, all mounted on a 10 Kelvin stage in a dewar with optical access. The goal of the system demonstration is to operate the superconductive A/D converter with 12 bit resolution at a rate of 10 mega samples per second at 10 K. The ADC chip will also be evaluated quantitatively to demonstrate digitization with no missing codes, low noise performance, and low power dissipation,

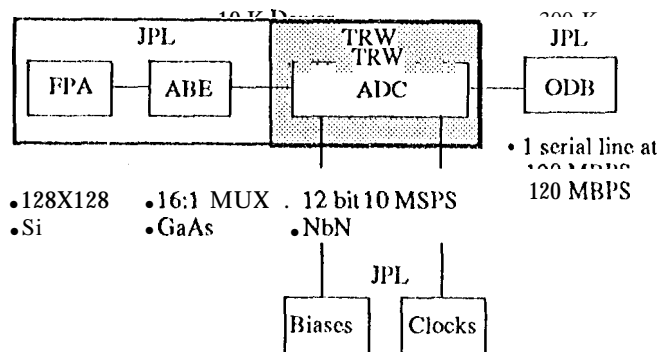


Figure 3: a block diagram of the joint JPL/TRW ASP demonstration showing the focal plane array (FPA), analog buffer electronics (ABE), analog-to-digital converter (ADC), and output digital buffer (ODB).

III. THE SUPERCONDUCTIVE ADC

The JPL/TRW IR ASP demonstration requires the ADC performance shown in Table I.

TABLE I
ASP DEMONSTRATION REQUIREMENT'S FOR THE ADC

ADC Requirement Specification	Expected Performance
conversion rate	10 mega samples per second
integration time	70 nsec
dynamic range	12 bits
operating temperature	10 K
quantizer thermal noise	< 1/2 LSB
	< 2% of reading over full dynamic range

We will meet these requirements using a single one-cm square integrated NbN superconductive circuit chip which includes an SFQ counting ADC similar to those demonstrated in Nb and an MVTL parallel to serial shift register to transmit the ADC data off chip using a single serial data line (see Figure 4). All of the circuits required for the demonstration integrated circuit chip, latching level and SFQ, have been demonstrated in Nb with large margins. In addition, we have reported an extensive study of our basic 10 Kelvin NbN MVTL gates which are to be used in the parallel to serial shift register[2]. Translation of SFQ designs from Nb to NbN is complicated by the reduced number of wire layers in the NbN process and the increased parasitic inductance of the NbN circuits. Our first translation from the Nb to NbN layout produced chips with working parallel-to-serial shift registers but an ADC with margins too small for the chip to be used in the demonstration. We are presently in the process of fabricating and testing improved ADC designs.

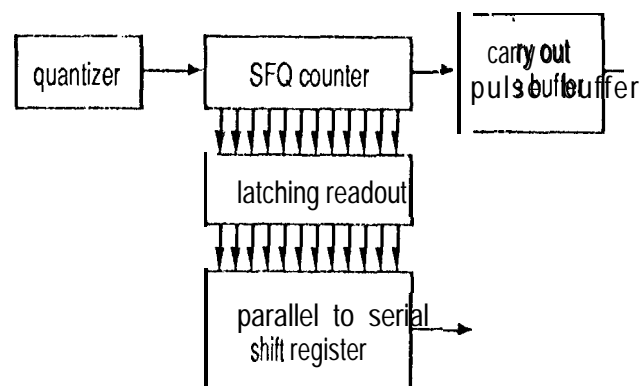


Figure 4: NbN integrated superconductive circuit chip block diagram. In the standard operating mode a single line transmits the digital data to the room temperature digital signal processing electronics.

The SFQ ADC, shown in Figure 5, consists of a quantizer SQUID, a gate SQUID, and a counter made up of a string of flip flop SQUIDS. In the voltage-to-frequency mode

of operation the quantizer SQUID is biased in the voltage slate using the gate bias current. The average quantizer voltage is measured by counting the total number of SFQ pulses it emits during the integration time defined by the time the gate is open. The signal current is magnetically coupled to the quantizer SQUID using a pick-up coil and modulates its voltage (see Figure 6). The operating point of the quantizer SQUID is set using the control line and gate bias line. The control line is adjusted so that in the absence of signal current the flux in the SQUID is approximately $(1/4)\Phi_0$ and then the gate bias current is set to bias the SQUID to a voltage corresponding to the low end of the signal range (approximately 30 nV for the 10 K ASP demonstration).

- SFQ ADC Block Diagram -

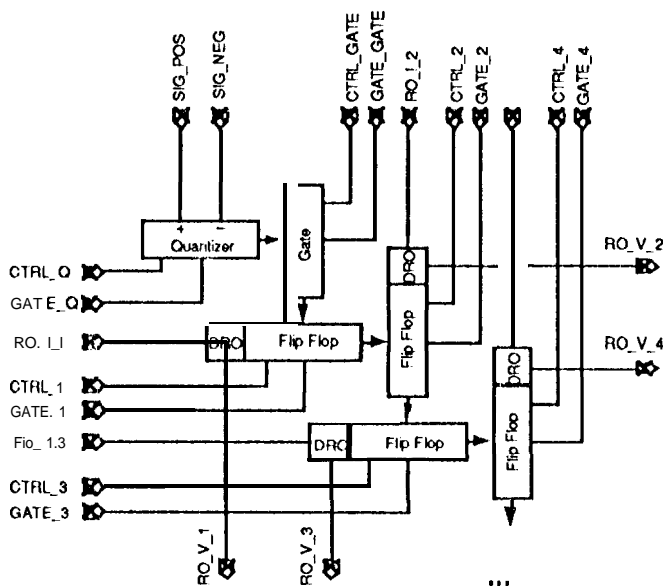


Figure 5: Block diagram of the SFQ ADC portion of the NbN integrated ADC chip. The functional blocks are shown in a realistic configuration showing the alternating orientation of the flip flop SQUIDS. Lines at the perimeter with inward pointing pin designators are input and control lines while those with outward pointing pins are voltage output lines. The pin designators and labels are used in TRW'S CAD system to perform automated schematic vs. layout verification.

To produce a chip with sufficient margins we have implemented reductions in the fabrication design rules and significant improvements in the layout. The reductions in design rules average approximately 40% and will directly lead to about a 25% reduction in parasitic inductance. We are in the process of fabricating and testing chips of the improved design.

Beyond producing a fully functional integrated chip, the ADC must meet two quantitative requirements: 1) the maximum counting frequency must be high enough to meet the required dynamic range and conversion rate, and 2) the thermal noise introduced by the quantizer must not limit the dynamic range or contaminate the signal.

A full scale signal must produce $\sim 2^N$ pulses out of the quantizer during the conversion time, t , where N is the

number of bits of resolution of the ADC. For $t = 70$ nsec and $N = 12$, this demonstration will require a frequency of 60 GHz. The maximum counting frequency is determined by the dynamics of the quantizer, the dynamics of the first flip flop, and the impedance of the connection between them. Our existing counters function to about 20 GHz. We have implemented design changes to improve each of these factors. Reduced parasitic inductance in our latest design will increase the maximum counting frequency. Counting frequencies above 60 GHz have been demonstrated for Nb SFQ counters at 4.2K [3]. We expect counters of our latest design to operate up to 60 GHz and meet the demonstration requirement.

- QUANTIZER SQUID -

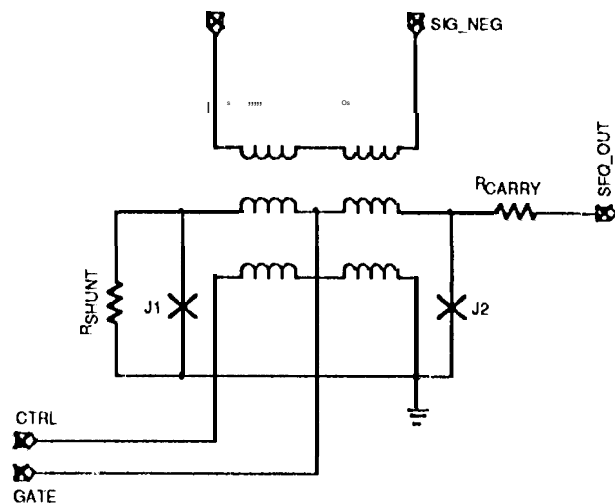


Figure 6: details of the quantizer SQUID. The pin designators are analogous to those in Figure 5. The junctions are not shunted except by the resistors explicitly shown.

After careful consideration we have determined that our NbN quantizer SQUIDS will meet the ADC noise requirement. The quantizer SQUID'S shunting resistors will add a thermally generated noise voltage to that representing the signal. To achieve a dynamic range of 12 bits the quantizer SQUID'S voltage noise must be smaller than the signal voltage at the low end of the range which, for the demonstration conditions, is 30 nV.

A simple model leads to the result that the Johnson noise voltage of a shunted junction is given by $V_{n,JJ} = (R_{DYN}/R_{SH}) V_n$, where V_n is the Johnson noise of the ohmic shunting resistor, R_{SH} , into a high impedance load, and R_{DYN} is the dynamic resistance of the shunted junction. The appropriate bandwidth for calculation of the Johnson noise voltage is the $(1/2t)$ where t is the ADC integration time (the SFQ counter acts as a low pass filter). Using $t = 70$ nsec, a one ohm shunting resistor at 10K generates a V_n of 63 nV. This would cause a problem if R_{DYN} was always at least as large as R_{SH} , as it is in the zero temperature resistively shunted junction model. Noise rounding of the quantizer current-voltage curve greatly reduces R_{DYN} at low voltages preventing the observation of large

voltage noise. Previous work at TRW on Nb counting ADCS has provided us with a detailed understanding of the shape of the quantizer SQUID I-V curve and R_{DYN} .

In our previous study, the quantizer of a Nb counting-type ADC was flux biased at an integral flux quantum and the voltage was measured as a function of gate bias current using the counter. This technique enabled the measurement of voltages far below 10 nV. Figure 7 shows the shape of a quantizer SQUID I-V curve for low voltages. The data points are fit in two regions by closed form expressions for the voltage as a function of gate bias current. The data above 4 μ V is fit well by $V = I_C R_{SH} ((I/I_C)^2 - 1)^{1/2}$. (Figure 8 dots not show all the data points, which extend to about 30 μ V. The RSJ form fits all the data above about 4 μ V.) The fit below 2 μ V is that given by V. Ambegaokar and B.I. Halperin [4]. In both cases I_C and R_{SH} are the only adjustable parameters. The two fits require slightly different values for I_C and R_{SH} (the fit below 2 μ V uses $I_C = 0.2443$ mA and $I_C R_{SH} = 55.0$ μ V, the fit above 3 μ V uses $I_C = 0.243$ mA and $I_C R_{SH} = 47.0$ μ V). The maximum R_{DYN} is 2.0 Ω , occurring in the cross-over region between 3 and 4 μ V. For small voltages R_{DYN} becomes much less than 1 Ω reducing the noise voltage far below that which would be present for the isolated shunting resistor. Note that the signal is input through the pick-up coil and this changing R_{DYN} does not change the input impedance of the ADC.

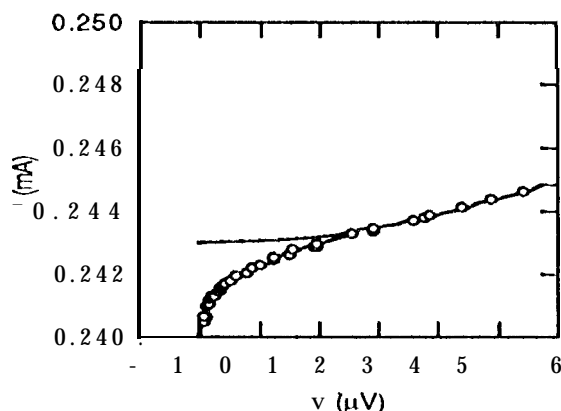


Figure 7: voltage corresponding to the measured quantizer frequency of a Nb ADC at 4.2K as a function of gate bias current for a zero magnetic flux bias (points). The upper solid line is the voltage vs. current curve expected for a resistively shunted junction (or SQUID with zero flux) at zero temperature and in the limit of small junction capacitance. I_C and R_n are adjusted to best fit the data, some of which is off scale. The lower solid curve is a fit to the rounding with I_C and R_n adjusted to best fit the data. The largest value for R_{DYN} ($= dV/dI$) is 2 Ω occurring in the cross over region between 2 and 4 μ V.

Direct measurement of the Nb ADC noise as a function of quantizer SQUID voltage confirms that Johnson noise is small enough to permit more than 12 bits of dynamic range. We read the SFQ counter a number of times for a given

quantizer SQUID gate current. The normalized standard deviation in the count is plotted as a function of quantizer SQUID voltage in Figure 8, expressed as a percent of reading. This is an unusual case where the Johnson noise depends on the signal voltage.

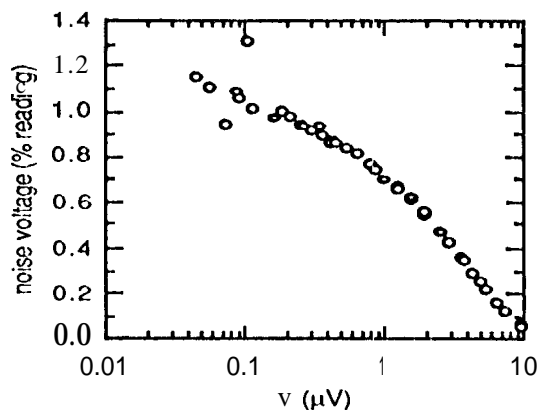


Figure 8: standard deviation of ADC count of a Nb ADC at 4.2K expressed as a per cent of the count as a function of the voltage corresponding to the average count. The variation due to quantizer voltage noise is less than 1.5 % over the entire operating range (30 nV and above).

The net result is that this noise mechanism will not limit the dynamic range or contribute a significant amount to the system noise.

The NbN ADC under development will meet all the requirements for integration into the JPL/TRW ASP demonstration and will prove the feasibility of this approach.

ACKNOWLEDGMENT

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